WHAT IS CLAIMED IS:

1. An integrated circuit testing method comprising:

a reading step wherein circuit data is read out by a circuit data reading unit;

a path cut step wherein a path cut point is selected from a target circuit and a state is fixed by a path cut countermeasure unit; and

an automatic test pattern generating step wherein test data to detect a delay failure with respect to the circuit whose path cut has been finished as a target is generated by an automatic test pattern generation unit,

wherein said automatic test pattern generating step comprises:

a narrowing step wherein an area including a sending FF group corresponding to failure presumption points, a receiving FF, and further, a preparation FF group that is one-stage precedent to said sending FF group is specified as a processing target circuit by a narrowing processing unit;

a failure exciting step wherein states of failure excitation at sending time and receiving time which have an inverting relation such that the state changes from 0 to 1 in a leading failure and changes from 1 to 0 in a trailing failure are allocated to said failure presumption points by a failure exciting

unit;

a path activating step wherein states at the sending time and the receiving time for activating a propagating path of said failure are allocated to the residual preparation FFs and sending FFs by a failure propagating state setting unit; and

a failure propagating step wherein, by an automatic test pattern generation control unit, a system clock is supplied as a sending clock to said sending FF, a change is given to a network from the sending FF and propagated, the system clock is supplied as a receiving clock to said receiving FF, and the network change is captured, thereby propagating a state for detecting the delay failure to a path between the sending FF and the receiving FF and generating a test pattern when the propagation succeeds, and further,

in said path activating step, an allocation of a don't care X is permitted as a state for activating the propagating path of the failure, and

in said failure propagating step, after the change in network, the state is transferred from the don't care X to an uncontrol value, thereby activating the propagating path of the failure.

2. A method according to claim 1, wherein said don't care X is a logic value constructing the test

pattern which does not exert an influence on a failure detection ratio even if it is replaced with an opposite value.

3. A method according to claim 1, wherein after said failure propagating step is finished, said method comprises:

a compaction failure exciting step wherein the don't care X in said path activating step changes to a value opposite to that of the state at the receiving time and the state of the failure excitation is allocated; and

a compaction failure propagating step wherein the system clock is supplied as a sending clock to said sending FF, the change is given to the network from the sending FF and propagated, the system clock is supplied as a receiving clock to said receiving FF, and the network change is captured, thereby propagating the state for detecting the delay failure to the path between the sending FF and the receiving FF and generating the test pattern when the propagation succeeds.

4. A method according to claim 1, wherein in said failure exciting step, when a clock-off is allocated to the sending FF at the sending time, an uncontrol value (u) showing that the failure excitation is

impossible for a failure value is conditional-implicated in an output of said sending FF at the receiving time, the allocation itself of said uncontrol value (u) is determined that the failure excitation is impossible, and the failure is excluded from targets of the delay failure.

5. A method according to claim 1, wherein when the failure propagation fails in said failure propagating step, among the failures which are presumed into the network from the network in which the failed failure has been presumed to a branch input of a fan-out free area, the failure in which the inverting relation is equal to that of the failed failure and a failure value is equal to a control value of a gate is extracted and excluded as an undetectable failure.

6. A method according to claim 1, wherein in said path cut step, in a gate input of driving the path cut point, a control value of a gate is given at the sending time and the receiving time and the state is fixed, or the uncontrol value of the gate is given to all gate inputs at the sending time and the receiving time and the state of said path cut point is fixed by allocating a fixed state "from 0 to 0" or "from 1 to 1".

7. A method according to claim 6, wherein said path cut step has a fixed state selecting step wherein, with respect to the fixed state "from 0 to 0" or "from 1 to 1" which is allocated to the path cut point, a failure detection impossible number is measured by said automatic test pattern generating step and the fixed state whose failure detection impossible number is small is selected.

8. A method according to claim 6, wherein said path cut step has a hazard-freeing step wherein in the case where a transfer in which a pin input position of the control value changes at the sending time and the receiving time exists among a plurality of input pins of the driver side gates for the path cut point, by adding and allocating the control value at the sending time to at least one input pin to which the control value is given at the receiving time, the hazard-free fixed state is generated for the path cut point.

9. A method according to claim 1, wherein in said narrowing step, as a preparation of said failure exciting step, a narrowing range is marked by back traces of two stages from the failure presumption point to the sending FF group via the receiving FF and from the sending FF group to the preparation FF

group, and if both states at the sending time and the receiving time of the network are not the don't care X, the back trace after the network is stopped.

10. A method according to claim 9, wherein in said automatic test pattern generating step, if the detection of the delay failure fails with respect to either the leading delay failure or the trailing delay failure of the same network, the unmarking of the narrowing range which has been marked by the back trace in said narrowing step is not performed but the mark is used as it is, and the test pattern generation is executed by using the other undetected delay failure as a target.

11. A program for allowing a computer to execute:

a reading step wherein circuit data is read out;

a path cut step wherein a path cut point is selected from a target circuit and a state is fixed by a path cut countermeasure unit; and

an automatic test pattern generating step wherein test data to detect a delay failure with respect to the circuit whose path cut has been finished as a target is generated,

wherein said automatic test pattern generating step allows the computer to execute:

a narrowing step wherein an area including a sending FF group corresponding to failure presumption points, a receiving FF, and further, a preparation FF group that is one-stage precedent to said sending FF group is specified as a processing target circuit;

a failure exciting step wherein states of failure excitation at sending time and receiving time which have an inverting relation such that the state changes from 0 to 1 in a leading failure and changes from 1 to 0 in a trailing failure are allocated to said failure presumption points;

a path activating step wherein states at the sending time and the receiving time for activating a propagating path of said failure are allocated to the residual preparation FFs and sending FFs; and

a failure propagating step wherein a system clock is supplied as a sending clock to said sending FF, a change is given to a network from the sending FF and propagated, the system clock is supplied as a receiving clock to said receiving FF, and the network change is captured, thereby propagating a state for detecting the delay failure to a path between the sending FF and the receiving FF and generating a test pattern when the propagation succeeds,

and further, in said path activating step, an allocation of a don't care X is permitted as a state for activating the propagating path of the failure,

and

in said failure propagating step, after the change in network, the state is transferred from the don't care X to an uncontrol value, thereby activating the propagating path of the failure.

12. A program according to claim 11, wherein said don't care X is a logic value constructing the test pattern which does not exert an influence on a failure detection ratio even if it is replaced with an opposite value.

13. A program according to claim 11, wherein after said failure propagating step is finished, said program allows the computer to execute:

a compaction failure exciting step wherein the don't care X in said path activating step changes to a value opposite to that of the state at the receiving time and the state of the failure excitation is allocated; and

a compaction failure propagating step wherein the system clock is supplied as a sending clock to said sending FF, the change is given to the network from the sending FF and propagated, the system clock is supplied as a receiving clock to said receiving FF, and the network change is captured, thereby propagating the state for detecting the delay failure

to the path between the sending FF and the receiving FF and generating the test pattern when the propagation succeeds.

14. A program according to claim 11, wherein in said failure exciting step, when a clock-off is allocated to the sending FF at the sending time, an uncontrol value showing that the failure excitation is impossible for a failure value is conditional-implicated in an output of said sending FF at the receiving time, an allocation itself of said uncontrol value is determined that the failure excitation is impossible, and the failure is excluded from targets of the delay failure.

15. A program according to claim 11, wherein when the failure propagation fails in said failure propagating step, among the failures which are presumed into the network from the network in which the failed failure has been presumed to a branch input of a fan-out free area, the failure in which the inverting relation is equal to that of the failed failure and a failure value is equal to a control value of a gate is extracted and excluded as an undetectable failure.

16. A program according to claim 11, wherein in

said path cut step, in a gate input of driving the path cut point, a control value of a gate is given at the sending time and the receiving time and the state is fixed, or the uncontrol value of the gate is given to all gate inputs at the sending time and the receiving time and the state of said path cut point is fixed by allocating a fixed state "from 0 to 0" or "from 1 to 1".

17. A program according to claim 16, wherein said path cut step has a fixed state selecting step wherein, with respect to the fixed state "from 0 to 0" or "from 1 to 1" which is allocated to the path cut point, a failure detection impossible number is measured by said automatic test pattern generating step and the fixed state whose failure detection impossible number is small is selected.

18. A program according to claim 16, wherein said path cut step has a hazard-freeing step wherein in the case where a transfer in which a pin input position of the control value changes at the sending time and the receiving time exists among a plurality of input pins of the driver side gates for the path cut point, by adding and allocating the control value at the sending time to at least one input pin to which the control value is given at the receiving

time, the hazard-free fixed state is generated for the path cut point.

19. A program according to claim 11, wherein in said narrowing step, as a preparation of said failure exciting step, a narrowing range is marked by back traces of two stages from the failure presumption point to the sending FF group via the receiving FF and from the sending FF group to the preparation FF group, and if both states at the sending time and the receiving time of the network are not the don't care X, the back trace after the network is stopped.

20. A program according to claim 19, wherein in said automatic test pattern generating step, if the detection of the delay failure fails with respect to either the leading delay failure or the trailing delay failure of the same network, unmarking of the narrowing range which has been marked by the back trace in said narrowing step is not performed but the mark is used as it is, and the test pattern generation is executed by using the other undetected delay failure as a target.

21. A computer-readable storing medium program for allowing a computer to execute:

a reading step wherein circuit data is read

out;

a path cut step wherein a path cut point is selected from a target circuit and a state is fixed by a path cut countermeasure unit; and

an automatic test pattern generating step wherein test data to detect a delay failure with respect to the circuit whose path cut has been finished as a target is generated,

wherein said automatic test pattern generating step allows the computer to execute:

a narrowing step wherein an area including a sending FF group corresponding to failure presumption points, a receiving FF, and further, a preparation FF group that is one-stage precedent to said sending FF group is specified as a processing target circuit;

a failure exciting step wherein states of failure excitation at sending time and receiving time which have an inverting relation such that the state changes from 0 to 1 in a leading failure and changes from 1 to 0 in a trailing failure are allocated to said failure presumption points;

a path activating step wherein states at the sending time and the receiving time for activating a propagating path of said failure are allocated to the residual preparation FFs and sending FFs; and

a failure propagating step wherein a system clock is supplied as a sending clock to said sending

FF, a change is given to a network from the sending FF and propagated, the system clock is supplied as a receiving clock to said receiving FF, and the network change is captured, thereby propagating a state for detecting the delay failure to a path between the sending FF and the receiving FF and generating a test pattern when the propagation succeeds,

and further, in said path activating step, an allocation of a don't care X is permitted as a state for activating the propagating path of the failure, and

in said failure propagating step, after the change in network, the state is transferred from the don't care X to an uncontrol value, thereby activating the propagating path of the failure.

22. An integrated circuit testing apparatus comprising:

a circuit data reading unit which reads out circuit data;

a path cut countermeasure unit which selects a path cut point from a target circuit and fixes a state; and

an automatic test pattern generation unit which generates test data to detect a delay failure with respect to the circuit whose path cut has been finished as a target,

wherein said automatic test pattern generation unit comprises:

a narrowing unit which specifies an area including a sending FF group corresponding to failure presumption points, a receiving FF, and further, a preparation FF group that is one-stage precedent to said sending FF group as a processing target circuit;

a failure exciting unit which allocates states of failure excitation at sending time and receiving time which have an inverting relation such that the state changes from 0 to 1 in a leading failure and changes from 1 to 0 in a trailing failure to said failure presumption points;

a failure propagating state setting unit which allocates states at the sending time and the receiving time for activating a propagating path of said failure to the residual preparation FFs and sending FFs; and

an automatic test pattern generation control unit which supplies a system clock as a sending clock to the sending FF, gives a change to a network from the sending FF and propagates the change, supplies the system clock as a receiving clock to said receiving FF, and captures the network change, thereby propagating a state for detecting the delay failure to a path between the sending FF and the receiving FF and generating a test pattern when the

propagation succeeds,

and further, said failure propagating state setting unit permits an allocation of a don't care X as a state for activating the propagating path of the failure, and

said automatic test pattern generation control unit transfers the state from the don't care X to an uncontrol value after the change in network, thereby activating the propagating path of the failure.